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Amendments To The Claims

Please cancel Claims 4-5, 7, 11-12 and 14 without prejudice. The following list of the claims replaces all prior versions and lists of the claims in this application.

1. (Currently amended) A method for the planarization of an integrated circuit structure emprising; comprising:

providing a substrate having a plurality of patterned regions;

polishing said substrate with an initial chemical mechanical polishing slurry until partial planarization occurs; and

continuing to final planarization with a second slurry;

wherein said initial slurry comprises a diluted ceria-based slurry with the compositions that ranges from 0.5 wt. % to 1.0 wt. % ceria; and

wherein said second slurry comprises a ceria-based slurry with composition ranging from 1.0 wt. % to 2.0 wt. % ceria, said initial slurry and said second slurry having different concentrations of ceria.

- 2. (Original) The method of claim 1 wherein said integrated circuit structure comprises shallow trench isolation.
- 3. (Original) The method of claim 2 wherein said shallow trench isolation comprises silicon oxide, silicon nitride and polysilicon layers in various configurations.

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- 4. (Canceled).
- 5. (Canceled).
- 6. (Original) The method of claim 1 wherein said polishing said substrate with said initial chemical mechanical polishing slurry until partial planarization occurs comprises a control of polishing time so as to avoid overpolishing of a stop layer.
 - 7. (Canceled).
- 8. (Original) The method of claim 1 wherein said continuing to final planarization with said second slurry completes said planarization.
- 9. (Currently amended) A method for the planarization of an integrated circuit structure emprising; comprising:

providing a substrate having a plurality of patterned regions wherein said substrate is to be planarized to a stop layer;

polishing said substrate with a first chemical mechanical polishing slurry composition until partial planarization occurs; and

thereafter continuing to final planarization with a second slurry;

wherein said first slurry comprises a diluted ceria-based slurry with compositions ranging from 0.5 wt. % to 1.0 wt. % ceria

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wherein said second slurry comprises a ceria-based slurry with composition ranging from 1.0 wt. % to 2.0 wt. % ceria, said first and second slurries having different concentrations of ceria.

- 10. (Original) The method of claim 9 wherein said integrated circuit structure comprises shallow trench isolation comprising silicon oxide and wherein said stop layer comprises one or more silicon nitride or polysilicon layers.
 - 11. (Canceled).
 - 12. (Canceled).
- 13. (Original) The method of claim 9 wherein said polishing said substrate with said first chemical mechanical polishing slurry composition until partial planarization occurs further comprises a control of polishing time so as to avoid overpolishing of said stop layer.
 - 14. (Canceled).
- 15. (Currently amended) A method for the planarization of an integrated circuit structure comprising:

providing a substrate having a plurality of patterned regions wherein said substrate is to be planarized to a stop layer;

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polishing said substrate with a diluted chemical mechanical polishing slurry composition and controlling polishing time so that said stop layer is not exposed; and

thereafter continuing to final planarization to said stop layer with a more concentrated composition of said chemical mechanical polishing slurry.

- 16. (Original) The method of claim 15 wherein the integrated circuit structure comprises shallow trench isolation.
- 17. (Original) The method of claim 16 wherein said shallow trench isolation comprises silicon oxide and wherein said stop layer comprises one or more silicon nitride or polysilicon layers.
- 18. (Original) The method of claim 15 wherein said diluted slurry comprises a diluted ceria-based slurry with compositions ranging from 0.5 wt. % to 1.0 wt. % ceria.
- 19. (Currently amended) The method of claim 15 wherein said more concentrated slurry composition consists of comprises a ceria-based slurry with composition ranging from 1.0 wt. % to 2.0 wt. % ceria.